LIVEWIRE™
FOR LIVE CAREERS

IC design & Verification - Internship

Days: 3 days **Duration: 15Hrs**

Day	Topics
1	**IC Design** Introduction to VLSI, Overview of the Software tool (cadence- Incisive Simulator): Working folder creation (myfolder, run, ts) , License activation commands , Basic Linux commands ,Code simulation commands , Types of modeling : Gate level modeling : Examples like Half adder, Full adder.
2	Structural modelling: Generation of one code from another code, Designing Four bit adder, Designing Four bit Multiplier
3	**IC Verification** Enum data type, Class ,Class randomization, Explicit coverage analysis, Verification of Behavioral model of ALU using class randomization and explicit coverage concept.